A 1GBIT/S OPTICAL/ELECTRICAL INPUT MONOLITHIC GaAs TRANSMITTER I.C.

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ABSTRACT

A 1GBit/s optical input transmitter chip has been developed to evaluate the performance of optical fibers as a communication media in high speed electronics. The transmitter chip has been fabricated in depletion mode GaAs with a one micron gate length. Optical/electrical functionality has been demonstrated at the wafer level.

INTRODUCTION

There is a growing demand to increase the throughput of high-speed processors and computers. To meet this demand, denser, higher speed IC's (VHSIC, VLSI, GaAs), and special purpose computer architectures (Systolic arrays, distributed processors etc.) are being developed. In increasing the system speed, high clock speeds and data rates are required which will require the interconnection between devices in a system to be improved. Conventional electrical interconnects are limited in speed due to the reactances of chip carriers and printed wiring boards. The problem is that both theory and some initial experiments indicate that the electrical reactances in the chip carrier and on the printed wiring board set a minimum of about 100 psec on the rising and falling edges of digital signals. Therefore, it is wise to investigate other interconnect technologies.

Optical interconnects have the potential to overcome some of the limitations of electrical interconnects. Optical communication has been demonstrated to have very large bandwidths on the order of tens of gigabits per second. In addition, there is virtually no cross talk between adjacent optical channels. There is no impedance matching required and there is no sensitivity to EMI.

With these characteristics, optical interconnects have the potential to assist in realizing the full potential of high speed circuits and systems by providing a high bandwidth interconnect. In this paper, we will describe the development of a GaAs transmitter chip which is an integral component required to implement a high speed monolithic optical interconnect.

We will also describe the packaging required to incorporate the optical and electrical interconnects into a single chip carrier.

DESIGN OF THE TRANSMITTER I.C.

The transmitter I.C. is the vehicle we will use to show the advantages of using optical interconnection for chip-to-chip and board-to-board communications.

The transmitter chip has been designed to digitally multiplex two electrical signal and two optical signals into a single output signal. The chip consists of two detectors (back-to-back Schottky diode detectors), two amplifiers, a 4:1 multiplexer and a laser driver. This design was implemented in a one micron depletion mode GaAs process using CML logic. Some of the typical processing parameters are listed below.

V_T = -1.1 volt
g_m = 110 mS/mm
g_{ds} = 10 mS/mm

The electrical data inputs to the transmitter chip undergo an on chip voltage translation before they are received by the 4:1 multiplexer. The optical data inputs to the transmitter chip are converted into a current by the on-chip detectors and is then translated into a voltage by the on-chip amplifiers before they are received by the 4:1 multiplexer. The amplifier used to translate the current into a voltage consists of three stages: a preamplifier, a gain and a buffer stage. The preamplifier translates the current into a voltage, its output is then amplified to the proper levels by the gain stage, and the buffer stage is used as a line driver to drive the input of the 4:1 multiplexer. The preamplifier uses a diode string on its input to translate the current from the detector into a voltage using the following equation:

$$V = 2V_t\, N\, \ell n \left(\frac{I_p}{I_{bias}} + 1 \right)$$

N = number of diodes in the string
I_{bias} = D.C. bias current
I_p = A.C. pulse current
V_t = K T/q

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The preamplifier has a gain of 20dB. There is feedback around the second stage of the preamplifier to improve its frequency response. [1]

A microphotograph of the complete transmitter chip is shown in Figure 4. The 4:1 multiplexer on this chip is implemented using a complementary clocked dual shift register architecture. This architecture makes it possible to have an output data rate (NRZ) that is twice the clock speed. All of the shift registers in the multiplexer were designed using a differential current-mode-logic structure to minimize the delay and device count in the shift registers. The complete transmitter chip consists of 807 depletion mode transistors and 325 level shifting diodes.

SYSTEM DESCRIPTION

The transmitter chip was designed to demonstrate the advantages of using optical interconnects for chip-to-chip and board-to-board communications. A breadboard test demonstration was designed to exercise the optical interconnects and test the functionality of the transmitter chip. A block diagram of our demonstration is shown in Figure 6. Four Fairchild 100K series shift registers provide 4 8-bit psuedo-random words at 250 MBit/sec. Two of the ECL chips are mounted with GaAs laser and drivers and are interconnected to the input of the transmitter chip via optical fibers. The other two word generators are connected electrically to the transmitter chip to provide a comparison to the optical interconnects. The 4:1 mux on the chip time multiplies the four inputs into a single 1 Gb/S data stream. The integrated laser driver is used to convert the digital levels into the current swings required to modulate a semiconductor laser. This demonstration will show the feasibility of using optical methods for interconnecting high speed digital devices and the capability of GaAs opto-integration methods for providing the required devices to implement high speed optical interconnects.

TEST RESULTS

Wafer level testing has been completed on the transmitter chip. The transmitter chip was found to be 100% functional at the wafer level electrical. An optical fiber was then positioned over one of the two detectors and one of the four data channels was successfully modulated with an optical input (see Figure 1). In Figure 1, B0, B1 and B2 are held constant and B3 is modulated on and off by the detector. The top trace is the serial data output from the multiplexer and the bottom trace is the clock output.

A custom package that will be used to test the optical and electrical inputs at high speed is presently being fabricated, high speed optical test data will be presented at the conference. A test fixture has been developed that has enabled us to run high speed electrical tests on the transmitter chip. High speed tests were performed to determine the maximum data rate that the 4:1 multiplexer on the transmitter chip is capable of handling. We found that the bandwidth of our test equipment was the limiting factor in determining the maximum data rate of the transmitter chip. The maximum data rate we were able to measure on the transmitter chip before test equipment failure was 2 Gbit/s (NRZ) (see Figure 2). At the 1 Gbit/s (NRZ) data rate that the transmitter chip was designed to operate at a (0111) input pattern was decoded at the output of the transmitter chip (see Figure 3). The transmitter chip is 2.82 x 2.04 $(mm)^2$ and it dissipated 3.5 watts of power at the 1 Gbit/s data rate.

PACKAGING

A custom package was designed to house both the GaAs transmitter chip and the four Si ECL word generator IC's. This package is a custom ceramic chip carrier with integral heat-sinking which drops into a mother board that provides system interconnections. Included on each chip carrier is provision for a laser diode and a laser-driver IC with a pig-tailed optical fiber. The chip carrier is designed to supply all the necessary optical, electrical, and thermal interfaces.

Package Construction

Organization of the package reflects that of the system block diagram shown in Figure 6. The GaAs transmitter chip and each of the four Si ECL word generator chips are packaged individually on five custom ceramic chip carriers. These chip carriers are a .010 inch by 1 inch square ceramic substrate soldered to a copper heatsink. The die are mounted to the heatsink through a hole in the ceramic. The chip carriers are interconnected with each other and with external systems by a mother board fabricated from Duroid 6010.5 substrate. Since the two types of substrate are the same thickness with similar dielectric constants, parasitic reactances at their interface are minimized.

The multimode optical fiber has a core diameter of 50 micrometers. A silicon die serves as a fixture to maintain alignment of the fiber end with the optical components. The fiber is laid into a V-groove etched in the silicon die and fastened with epoxy. A two-groove die simultaneously aligns two fibers with the two detectors on the GaAs transmitter chip, while a second silicon die beneath the fibers adjusts the height of the fibers above the detectors.

These V-grooved silicon die are also used to butt-couple two fibers together at a junction mounted on the mother board. Losses in this junction are only a few tenths of a dB. External optical connections are via 7 mm coaxial-type optical connectors.

The mother board is mounted on an aluminum plate which is housed in a test fixture. The chip carriers drop into wells through the mother board and into the plate to maintain alignment of the two dielectric substrates. The ground planes are kept continuous by a conductive O ring beneath the ceramic at its periphery. Gold ribbon fingers welded to the chip carrier lines contact corresponding lines on the mother board.

Optical Interface

The detectors shown in Figure 5 lie on the top surface of the GaAs IC. Light from the optical fibers is coupled to them through the sides of the fibers, the ends of the fibers are polished to a 58-degree angle. Total internal reflection from the end directs the light laterally through the side of the fiber. The fiber acts as a cylindrical lens to focus the light onto the detector.

Electrical Interface

Electrical interconnections in this multi-chip system are via micro-strip lines printed on the ceramic chip carriers and on the system mother board. The data rate of 1 Gigabit per second requires a controlled-impedance electrical environment to avoid radiative coupling and losses and ringing on the lines. This need is satisfied by the micro-strip lines and by providing a terminating impedance for all lines.

Control over propagation delays is a second major constraint in the layout of this system. Clocks and triggers to the four word-generator IC's and to the GaAs transmitter IC must be synchronous. In addition, the propagation delays from the word generators to the transmitter via micro-strip must be matched to those via the optical fibers.

Power line filtering is performed at three levels. EMI feedthroughs remove external signals from the power busses. In a bottom compartment to the test fixture 10 microfarad capacitors provide low-frequency filtering of switching transients. Lastly, 190 picofarad chip capacitors on the chip carrier perform the necessary high-frequency filtering.

CONCLUSION

In conclusion, a transmitter chip has been designed and shown to be functional at a 2 Gbit/s data rate. This transmitter will be used to quantitatively compare the performance of optical and electrical interconnects using one monolithic integrated GaAs circuit.

ACKNOWLEDGEMENTS

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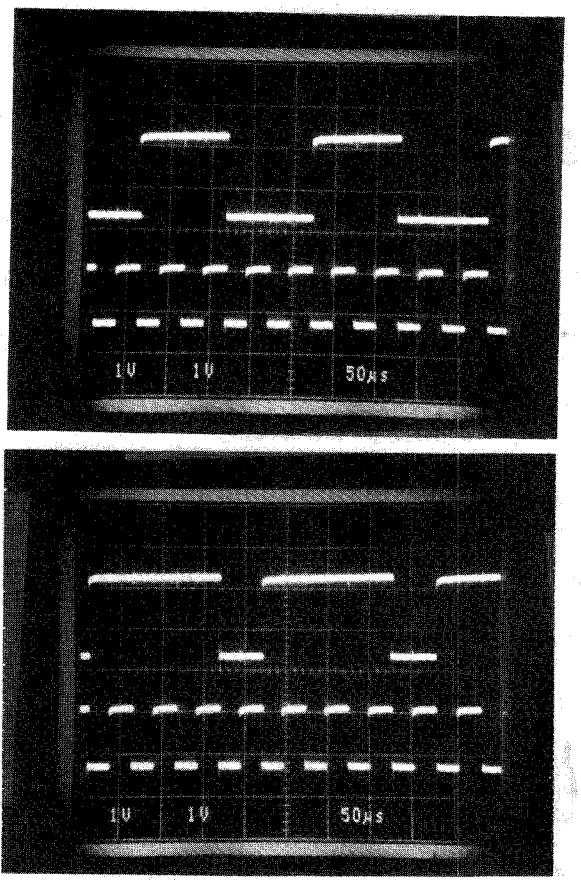

Figures 1a and 1b: Test results from wafer probing. In both figures B0, B1 and B2 are held at a fixed value, B3 was modulated on and off with an optical input. The top trace in both figures is the data output of the multiplexer and the bottom trace is the clock out of the multiplexer. B3 is off in the top figure (1a) and on in the bottom figure (1b).

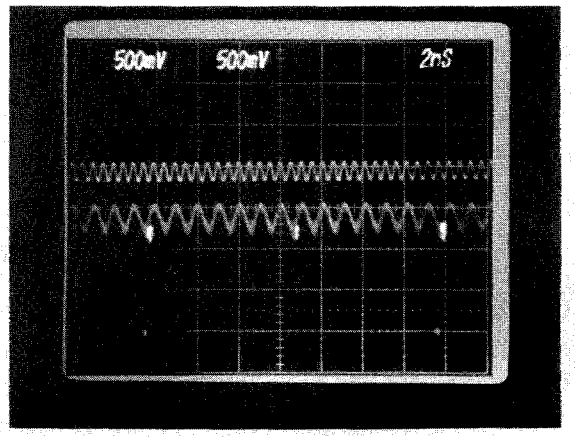

Figure 2: Output of the transmitter chip operating at a 2 Gbit/s data rate electrically. The top trace is the clock input signal and the bottom trace is the data output signal.

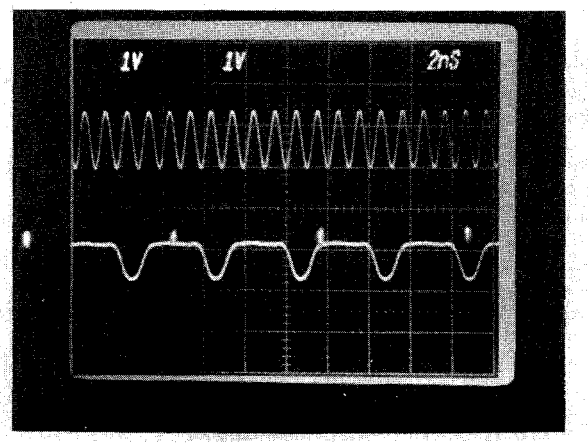

Figure 3: Output of the transmitter chip operating at a 1 Gbit/s data rate with a (0111) input pattern. The top trace is the clock input signal and the bottom trace is the data output signal.

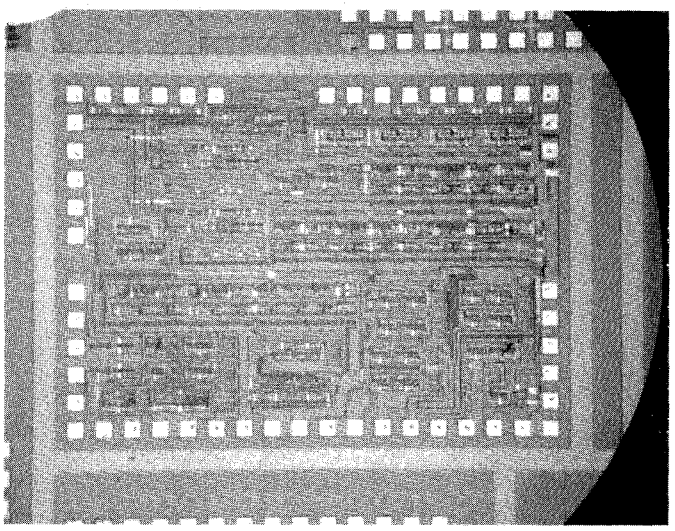

Figure 4: A microphotograph of the complete chip.

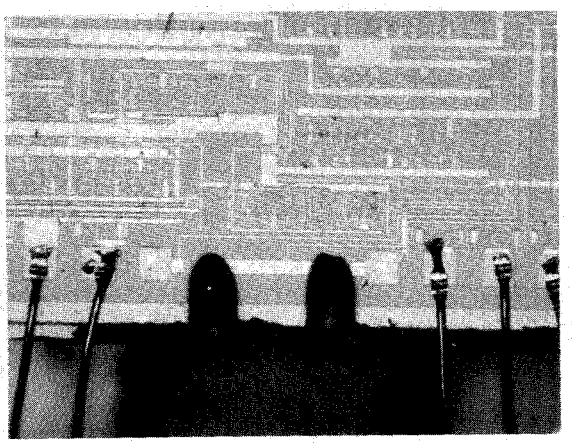

Figure 5: Shows the fiber alignment over the on-chip detectors.

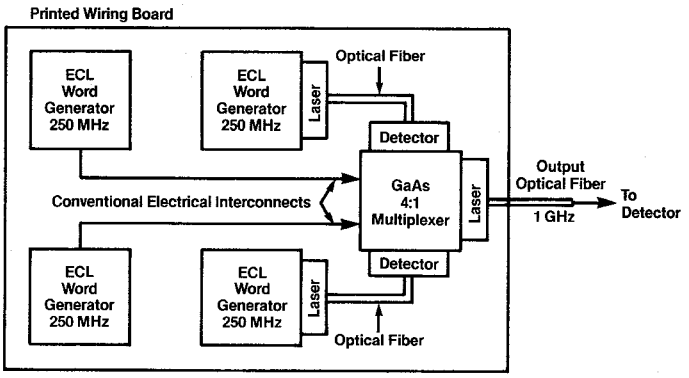

Figure 6: Block diagram of the optical chip to chip interconnect demonstration.